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PATENT ABSTRACTS OF JAPAN

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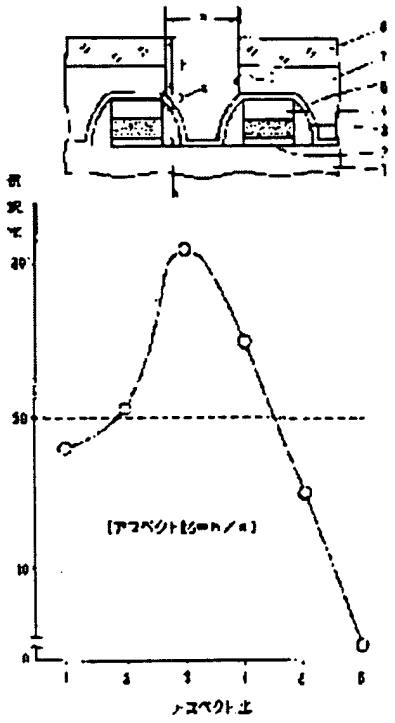
(54) MANUFACTURE OF SEMICONDUCTOR DEVICE

(57)Abstract:
PROBLEM TO BE SOLVED: To prevent degradation of dielectric strength and short circuit by preventing film reduction of an etching stopper layer at a self-align contact forming process.
SOLUTION: The shape, thickness and the like of an opening of a resist mask 8 is controlled such that an aspect ratio h/a including the thickness of the resist mask 8 for forming a self-align contact hole 9 is about greater than 2 and equal to or less than 4.5 above the shoulder of a side wall spacer 5. The etching selectivity between an interlayer insulating film of SiO2 or the like and the side wall spacer 5 of Si3N4 takes the maximum value when the aspect ratio including the thickness of the resist mask 8 is from about greater than 2 and equal to or less than 4.5. Accordingly, degradation of dielectric strength and short circuit can be prevented by employing the aspect ratio in this range.



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CLAIMS [Claim(s)]

[Claim 1] The process which forms two or more gate electrodes through a gate insulator layer on a semiconductor substrate, All over [aforementioned-on aforementioned gate insulator layer] two or more gate electrode top, anisotropic etching of the process and the aforementioned sidewall cambium which form a sidewall cambium is carried out. The process which forms a sidewall spacer in two or more aforementioned gate electrode sides, The process which forms an etching stopper layer in the whole surface, the process which forms a layer insulation film on the aforementioned etching stopper layer, The process and the aforementioned resist mask which form the resist mask which has opening which attends gate inter-electrode the semiconductor substrate and sidewall spacer of the aforementioned plurality on the aforementioned layer insulation film are used as an etching mask. In the manufacture method of a semiconductor device of having the process which carries out anisotropic etching of the aforementioned layer insulation film at least, and carries out opening of the self aryne contact hole An aspect ratio also including the thickness of the aforementioned resist mask of the aforementioned self aryne contact hole is the manufacture method of the semiconductor device characterized by being less than [more than abbreviation 2 4.5] in a part for the up shoulder of the aforementioned sidewall spacer.

[Claim 2] The opening flat-surface configuration of the aforementioned resist mask is the manufacture method of the semiconductor device according to claim 1 characterized by having two or more openings.

[Claim 3] It is the manufacture method of the semiconductor device according to claim 1 characterized by the aforementioned layer insulation film containing a silicon-oxide layer while the aforementioned etching stopper layer contains a silicon-nitride layer.

[Translation done.]

DETAILED DESCRIPTION [Detailed Description of the Invention]
[0001]
[The technical field to which invention belongs] this invention relates to the manufacture method of a semiconductor device of having the process which forms self aryne contact structure with high-reliability, in more detail about the manufacture method of a semiconductor device.
[0002]
[Description of the Prior Art] the high integration of semiconductor devices, such as LSI, and highly-efficient-izing -- progressing -- following -- a gate electrode and connection -- design rules, such as a hole, are also being reduced to less than [a quarter micron or it] In this semiconductor device, in order to avoid the various troubles which accompany high integration, also in the interlayer connection structure in a multilayer interconnection, much devices are taken on a layout or a process.
[0003] As the example, there are the alignment gap of an aligner and the problem of size deflection at the time of lithography. In the present aligner, the alignment precision gap at the time of mask alignment is the thing of 80nm and a scanning type in a stepper, and is said to be 50nm. for this reason -- for example, detailed contact hole formation gate inter-electrode [two or more] is becoming difficult
[0004] The method thought out in order to solve this problem is self aryne contact (Self Aligned Contact) technology. the connection which attends the impurity diffusion layer of two or more gate inter-electrode semiconductor substrates etc. when self aryne contact forms the sidewall spacer and the etching stopper layer in the sides, such as a gate electrode, -- a hole -- self -- it is the method of carrying out opening conformably The process which carries out alignment of the resist mask which has detailed opening to the connection hole opening schedule section strictly by adoption of self aryne contact becomes unnecessary. Moreover, since it becomes unnecessary [an alignment margin], reduction of a semiconductor chip or cell area is also attained.
[0005] The outline of the manufacture method of the conventional self aryne contact is explained with reference to drawing 5 and drawing 6 . As first shown in drawing 5 (a), the gate insulator layer 2, the gate electrode 3, and the offset insulator layer 4 are formed one by one on the semiconductor substrates 1, such as silicon. next the sidewall cambium (not shown) by the silicon oxide etc. is deposited on the whole surface, whole surface etchback of this is carried out, and it is shown in drawing 5 (b) -- as -- the sidewall spacer 5 -- the side of the gate electrode 3 and the offset insulator layer 4 -- leaving -- further -- the whole surface -- Si 3N4 etc. -- the etching stopper layer 6 is formed in conformal one In addition, before and after the formation process of the sidewall spacer 5, an impurity diffusion layer (not shown) is formed at the semiconductor substrate 1. As shown in drawing 5 (c) after this, the layer insulation films 7, such

as a silicon oxide, are formed in the whole surface, and patterning of the resist mask 8 further for self aryne contact openings is carried out. The exact alignment at the time of exposure of resist mask 8 patterning does not need strict nature so much. As furthermore shown in drawing 6 (d), anisotropic etching of the layer insulation film 7 is carried out by using the resist mask 8 as an etching mask. Under the present circumstances, opposite Si 3N4 The high etching conditions of a selection ratio are adopted and etching is stopped on the etching stopper layer 6. Then, as shown in drawing 6 (e), the exposed etching stopper layer 6 is removed by wet etching, ionicity weak dry etching, etc., and the self aryne contact hole 9 which attends the impurity diffusion layer of the semiconductor substrate 1 is completed.

[0006] The outline plan of self aryne contact hole 9 portion which removed the etching stopper layer 6 and was completed is shown in drawing 6 (e). It has the position and width of face which were regulated by the self-adjustment target with the sidewall spacer 5, and opening of the pars basilaris ossis occipitalis of the self aryne contact hole 9 can also be considered as the minute opening width of face below the resolution limit of lithography.

[0007]

[Problem(s) to be Solved by the Invention] The technical key point in a self aryne contact process is Si 3N4 used as an etching stopper layer. SiO2 with the receiving high selection ratio It is adoption of etching conditions. Etching removal of the etching stopper layer is carried out to this selection ratio being insufficient, the sidewall spacer exposed from the etching stopper layer and an offset insulator layer carry out film decrease, and, as a result, the fall of a contact plug / gate inter-electrode pressure-proofing and faults, such as a short circuit, arise.

[0008] SiO2 / Si 3N4 As a method of raising the etch selectivity of a between, the method using the mixed gas which added CO is in the etching gas of CF system as reported to the collection p537 of the 41st applied-physics relation union lecture meeting (1994 spring annual conventions) lecture drafts, and lecture number 29 p-ZF -2. this -- SiO2 the ionicity in anisotropic etching -- to some extent -- suppressing -- mainly -- Si 3N4 a top -- carbon -- the protective coat by rich CF system polymer -- depositing -- SiO2 The fall of an etching rate is the method of obtaining a selection ratio, by adopting a high-density plasma etching system.

[0009] However, in the anisotropic etching of self aryne contact, there is a specific problem that it is large, namely, the etching rate of a selection ratio of the etching stopper layer 6 of the up shoulder of the sidewall spacer 5 is small as compared with the etching rate of the etching stopper layer 6 of a flat part. This is because sputtering removal of the CF system polymer which should be deposited on a sidewall spacer 5 up shoulder is carried out preferentially, when the vertical-incidence nature of ion is raised for anisotropic etching. This cause is made because, as for the sputtering efficiency by ion, an ion incident angle serves as the maximum at 40-60 degrees. If the ion mode nature in anisotropic etching is weakened or too much polymer deposition is formed in order to improve the selection ratio in etching stopper layer 6 portion on a sidewall spacer 5 up shoulder, the problem that etching stops at the contact hole pars basilaris ossis occipitalis of a high aspect ratio will newly occur.

[0010] Let it be the technical problem for this invention to solve the trouble of these conventional technology in the manufacture method of a semiconductor device including the self aryne contact formation process mentioned above. That is, the technical problem of this invention is Si 3N4 as an etching stopper layer. It sets to the manufacture method of a semiconductor device including used self aryne contact processing, and they are SiO2 / Si3N4. It is improving the selection ratio of a between and offering the manufacture method of the

semiconductor device in which the high anisotropic etching of a throughput is possible. Moreover, another technical problem of this invention is offering the manufacture method of a semiconductor device of having reliable self aryne contact structure without fear, such as a fall of isolation voltage, and a short circuit.

[0011]

[Means for Solving the Problem] this invention is made in order to attain the technical technical problem mentioned above. Namely, the process at which the manufacture method of the semiconductor device of this invention forms two or more gate electrodes through a gate insulator layer on a semiconductor substrate, All over two or more this gate insulator layer top and gates electrode top, anisotropic etching of the process and sidewall cambium which form a sidewall cambium is carried out. The process which forms a sidewall spacer in two or more previous gate electrode sides, The process which forms an etching stopper layer in the whole surface, the process which forms a layer insulation film on this etching stopper layer, The process which forms the resist mask which has opening which attends two or more previous gate inter-electrode semiconductor substrates and sidewall spacers on this layer insulation film, and this resist mask are used as an etching mask. In the manufacture method of a semiconductor device of having the process which carries out anisotropic etching of the layer insulation film at least, and carries out opening of the self aryne contact hole An aspect ratio also including the thickness of a resist mask of this self aryne contact hole is characterized by being less than [more than abbreviation 2 4.5] in a part for a sidewall spacer up shoulder.

[0012] The manufacture method of the semiconductor device of this invention may set like 1 operative condition, and the opening flat-surface configuration of this resist mask may have two or more openings. Moreover, in the manufacture method of the semiconductor device of this invention, while an etching stopper layer contains a silicon-nitride layer, a layer insulation film can be preferably applied, when a silicon-oxide layer is included.

[0013] It moves to explanation of the operation to the next. this invention person is SiO2 / Si 3N4 used as the key point in the anisotropic etching of self aryne contact. As a result of advancing examination wholeheartedly about the selection ratio of a between, the substantial aspect ratio including the thickness of the resist mask in a self aryne contact hole portion other than etching conditions, such as selection of a type of gas, found out influencing a selection ratio greatly. This relation is explained with reference to drawing 4 .

[0014] Drawing 4 is SiO2 / Si 3N4 at the time of self aryne contact opening. It is the graph which shows the selection ratio of a between, and the relation of an aspect ratio. Etching adopts a magnetron RIE system and etching gas is C4 F8 as CF system gas. The mixed gas containing CO was used. Moreover, the aspect ratio said here is the value of h/a which **(ed) the value of the distance h from a part for the up shoulder of the sidewall spacer 5 of the self aryne contact hole 9 (the portion S enclosed with the dotted-line circle of drawing 4) to the front face of the resist mask 8 with the value of the opening width of face a of the resist mask 8.

[0015] It turns out that an aspect ratio can attain 20 or more etch selectivity in not more than more than abbreviation 2 4.5 so that clearly from the graph of drawing 4 . If these high selection-ratio conditions are used, before dirty-off of the etching stopper layer 6 of S portion is carried out, it is possible enough to remove the layer insulation film 7 of self aryne contact hole 9 pars basilaris ossis occipitalis without a residue. Control of the value of this aspect ratio h/a is possible by the design of the diameter a of opening of the resist mask 8, thickness, or the thickness of a layer insulation film. Moreover, an aspect ratio becomes less than two from the

relation of device structure. In this case, what is necessary is to make the opening flat-surface configuration of the resist mask 8 into plurality, and just to control a substantial aspect ratio in the range not more than more than abbreviation 2 4.5 by reducing the diameter a of opening.
[0016]
[Example] Hereafter, with reference to an accompanying drawing, it explains about the concrete example of this invention. In addition, the same reference mark shall be given to the same component as the inside of drawing 5 with which explanation of the conventional technology was presented, and drawing 6 .
[0017] Example 1 this example uses the opening flat-surface configuration of a resist mask as single opening, controls an aspect ratio by controlling the thickness of a resist mask, and is SiO2 / Si 3N4. It is the example which improved the selection ratio of a between, and the drawing 1 reference is carried out and this is explained.
[0018] The structure of the processed substrate adopted by this example is the same as that of what was shown by drawing 5 (c) with which explanation of the conventional example was presented fundamentally. Namely, as the processed substrate adopted by this example is shown in drawing 1 (a) On the semiconductor substrates 1, such as silicon, for example, by thermal oxidation The gate insulator layer 2 and n+ which were formed in the thickness of 10nm two or more gate electrodes 3 with a thickness of 500nm it is thin from polycrystal silicon, and SiO2 from -- SiO2 of thickness with a width of face of 250nm formed in the side of the offset insulator layer 4 with a thin thickness of 500nm, the gate electrode 3, and the offset oxide film 4 from -- the becoming sidewall spacer 5 -- Were formed in the whole surface of reduced pressure CVD. Si 3N4 from -- SiO2 formed all over the etching stopper layer 6 with a thin thickness of 50nm It consists of a layer insulation film 7 which consists of a PSG etc., and a resist mask 8 for self aryne contact openings formed in the thickness of 1.2 micrometers. Patterning of the single opening of the diameter of 0.8 micrometer which attends the semiconductor substrate 1 between the sidewall spacer 5 and the sidewall spacer 5 is carried out to this resist mask, for example. The exact alignment at the time of exposure of this resist mask 8 patterning does not need strict nature so much. The thickness of the layer insulation film 7 is 800nm in the flat part for example, on the offset insulator layer 4, and flattening of the front face may be carried out by reflow heat treatment, chemical mechanical polishing, etc. Moreover, the distance between the gate electrodes 3 which plurality adjoins is 850nm.
[0019] As the processed substrate of this structure was etched two stages by the magnetron RIE system and it was shown in drawing 1 (b) according to the following etching conditions, the self aryne contact hole 9 was formed.
1st-step etching (etching of the layer insulation film 7) C4 F8 Flow rate 10 sccm CO flow rate 150 sccm Ar flow rate 200 sccm Gas pressure 5.3 Pa RF power 1600 W (13.56MHz) Processed substrate temperature The step [20 ** / 2nd step] etching (etching of the etching stopper layer 6) CHF3 Flow rate 20 sccm O2 Flow rate 20 sccm Gas pressure 2.7 Pa RF power 500 W (13.56MHz)
Processed substrate temperature 20 ** [0020] When the processed substrate adopted by this example forms the thickness of the resist mask 8 comparatively thickly with 1.2 micrometers, the aspect ratio of the self aryne contact hole 9 is designed in the sidewall spacer 6 shoulder upper part including the thickness of the resist mask 8 so that it may be set to 2.5. Therefore, SiO2/Si 3N4 in this portion The etch selectivity of a between is the highest field so that clearly from the graph of drawing 4 .

[0021] For this reason, also in the shoulder upper part of the sidewall spacer 5 which spatter out is the easiest to be carried out in the 1st-step etching, it does not generate, therefore neither the sidewall spacer 5 nor the offset insulator layer 4 carries out film decrease of the fault the etching stopper layer 6 disappears. The 2nd-step etching is ended and the flat-surface configuration of self aryne contact hole 9 portion after exfoliating the resist mask 8 is shown in drawing 1 (c). The semiconductor substrate 1 and the sidewall spacer 5 are exposed to self aryne contact hole 9 base. Then, the contact plug and the upper wiring which are not illustrated according to a conventional method are formed.

[0022] They are SiO2 / Si 3N4 by optimizing the thickness of the resist mask of a single opening flat-surface configuration according to this example. It is possible to manufacture the semiconductor device which has the self aryne contact hole which raised the etch selectivity of a between and was excellent in the configuration.

[0023] By using the opening flat-surface configuration of a resist mask as opening of the shape of two or more ellipse, example 2 this example controls an aspect ratio, and is SiO2 / Si 3N4. It is the example which improved the selection ratio of a between, and the drawing 2 reference is carried out and this is explained.

[0024] The structure of the processed substrate shown in drawing 2 (a) adopted by this example is the same as that of what was shown by drawing 5 (c) with which explanation of the conventional example was presented fundamentally. that is On the semiconductor substrates 1, such as silicon, by thermal oxidation The gate insulator layer 2 and n+ which were formed in the thickness of 10nm two or more gate electrodes 3 with a thickness of 500nm it is thin from polycrystal silicon, and SiO2 from -- SiO2 of thickness with a width of face of 200nm formed in the side of the offset insulator layer 4 with a thin thickness of 300nm, the gate electrode 3, and the offset oxide film 4 from -- the becoming sidewall spacer 5 -- SiO2 formed all over the etching stopper layer 6 with a thickness of 50nm formed in the whole surface of reduced pressure CVD By PSG etc. It consists of a formed layer insulation film 7 and a resist mask 8 for self aryne contact openings formed in the thickness of 0.5 micrometers. For example, it attends the semiconductor substrate 1 between the sidewall spacer 5 and the sidewall spacer 5, patterning of the two ellipse openings of the diameter of 0.8 micrometerx0.3 micrometer is carried out in parallel, and the slit between two openings has become 0.2 micrometers at this resist mask 8. The resist mask of this configuration can be formed with for example, a chemistry amplification resist and excimer laser lithography. The exact alignment at the time of exposure of this resist mask 8 patterning does not need strict nature so much. The thickness of the layer insulation film 7 is 400nm in the flat part for example, on the offset insulator layer 4. Moreover, the distance between the gate electrodes 3 which plurality adjoins is 1.0 micrometers.

[0025] The processed substrate of this structure was etched two stages according to the following etching conditions by the magnetron RIE system.

1st-step etching (etching of the layer insulation film 7) C4 F8 Flow rate 10 sccm CO flow rate 150 sccm Ar flow rate 200 sccm Gas pressure 5.3 Pa RF power 1600 W (13.56MHz) Processed substrate temperature The step [20 ** / 2nd step] etching (etching of the etching stopper layer 6) CHF3 Flow rate 20 sccm O2 Flow rate 20 sccm Gas pressure 2.7 Pa RF power 500 W (13.56MHz)

Processed substrate temperature 20 ** [0026] When the processed substrate adopted by this example divides the opening configuration of the resist mask 8 into plurality, the aspect ratio of the direction of a minor axis of self aryne contact hole 9 opening including the thickness of the

resist mask 8 is designed so that it may be set to 3.0 in the shoulder upper part of the sidewall spacer 5. Therefore, SiO2/Si 3N4 in this portion The etch selectivity of a between shows the highest value so that clearly from the graph of drawing 4 .

[0027] For this reason, also in the shoulder upper part of the sidewall spacer 5 which spatter out is the easiest to be carried out in the 1st-step etching, it does not generate, therefore neither the sidewall spacer 5 nor the offset insulator layer 4 carries out film decrease of the fault the etching stopper layer 6 disappears. The configuration of self aryne contact hole 9 portion after the 1st-step etching end is shown in drawing 2 (b). The etching stopper layer 6 was removed by the 2nd-step weak etching in ion mode after this, the resist mask 8 was exfoliated further, and the self aryne contact hole 9 was completed. The flat-surface configuration of self aryne contact hole 9 portion is shown in drawing 2 (c). The semiconductor substrate 1 and the sidewall spacer 5 are exposed to two self aryne contact hole bases of an ellipse.

[0028] The contact plug and the upper wiring which are not illustrated according to a conventional method after this are formed. Although the pillar of the slit-like layer insulation film 7 remains in the self aryne contact hole 9, unless trouble is caused to a contact plug and the step coverage at the time of formation of the upper wiring, you may leave as it is. Moreover, after isotropic etching etc. removes separately, you may form a contact plug and the upper wiring.

[0029] They are SiO2 / Si 3N4 by dividing the opening flat-surface configuration of a resist mask into two or more ellipses according to this example. It is possible to manufacture the semiconductor device which has the self aryne contact hole which raised the etch selectivity of a between and was excellent in the configuration.

[0030] By using the opening flat-surface configuration of a resist mask as concentric circle-like opening, example 3 this example controls an aspect ratio, and is SiO2 / Si 3N4. It is the example which improved the selection ratio of a between, and the drawing 3 reference is carried out and this is explained.

[0031] The structure of the processed substrate shown in drawing 3 (a) adopted by this example is the same as that of what was shown by drawing 5 (c) with which explanation of the conventional example was presented fundamentally. that is On the semiconductor substrates 1, such as silicon, by thermal oxidation The gate insulator layer 2 and n+ which were formed in the thickness of 10nm two or more gate electrodes 3 with a thickness of 500nm it is thin from polycrystal silicon, and SiO2 from -- SiO2 of thickness with a width of face of 200nm formed in the side of the offset insulator layer 4 with a thin thickness of 300nm, the gate electrode 3, and the offset oxide film 4 from -- the becoming sidewall spacer 5 -- SiO2 formed all over the etching stopper layer 6 with a thickness of 50nm formed in the whole surface of reduced pressure CVD By PSG etc. It consists of a formed layer insulation film 7 and a resist mask 8 for self aryne contact openings formed in the thickness of 0.5 micrometers.

[0032] As this resist mask 8 is shown in the opening flat-surface configuration shown in drawing 3 (b), it has circular opening with a diameter of 0.8 micrometers expected to the semiconductor substrate 1 between the sidewall spacer 5 and the sidewall spacer 5, and with a diameter of 0.2 micrometers resist pillar 8a is formed in the shape of a concentric circle. Therefore, concentric circle-like resist mask 8 opening width of face is 0.3 micrometers. The resist mask of this configuration can also be formed with a chemistry amplification resist and excimer laser lithography. The exact alignment at the time of exposure of this resist mask 8 patterning does not need strict nature so much. The thickness of the layer insulation film 7 is 400nm in the flat part for example, on the offset insulator layer 4. Moreover, the distance between the gate electrodes 3

which plurality adjoins is 1.0 micrometers.
[0033] As the processed substrate of this structure was etched two stages by the magnetron RIE system and it was shown in drawing 3 (c) according to the following etching conditions, the self aryne contact hole 9 was formed.
1st-step etching (etching of the layer insulation film 7) C4 F8 Flow rate 10 sccm CO flow rate 150 sccm Ar flow rate 200 sccm Gas pressure 5.3 Pa RF power 1600 W (13.56MHz) Processed substrate temperature The step [20 ** / 2nd step] etching (etching of the etching stopper layer 6) CHF3 Flow rate 20 sccm O2 Flow rate 20 sccm Gas pressure 2.7 Pa RF power 500 W (13.56MHz)
Processed substrate temperature 20 ** [0034] When the processed substrate adopted by this example makes the opening configuration of the resist mask 8 the shape of a concentric circle, the radial aspect ratio of the self aryne contact hole 9 including the thickness of the resist mask 8 is designed so that it may be set to 3.0 in the shoulder upper part of the sidewall spacer 5. Therefore, SiO2 / Si 3N4 in this portion The highest value is shown that the etch selectivity of a between is clear from the graph of drawing 4 .
[0035] For this reason, also in the shoulder upper part of the sidewall spacer 5 which spatter out is the easiest to be carried out in the 1st-step etching, it does not generate, therefore neither the sidewall spacer 5 nor the offset insulator layer 4 carries out film decrease of the fault the etching stopper layer 6 disappears. Then, the resist mask 8 after removing the etching stopper layer 6 is exfoliated by the 2nd-step etching, and the contact plug and the upper wiring which are not illustrated according to a conventional method are formed. Although the pillar of the circular layer insulation film 7 remains in the self aryne contact hole 9, unless trouble is caused to a contact plug and the step coverage at the time of formation of the upper wiring, you may leave as it is. Moreover, after isotropic etching etc. removes separately, you may form a contact plug and the upper wiring.
[0036] They are SiO2 </SUB> / Si 3N4 by making the opening flat-surface configuration of a resist mask into the shape of a concentric circle according to this example. It is possible to manufacture the semiconductor device which has the self aryne contact hole which raised the etch selectivity of a between and was excellent in the configuration.
[0037] As mentioned above, although the example of three examples explained this invention in detail, this invention is not limited to these examples at all. That is, the thickness of the resist mask in an example or a layer insulation film, the diameter of opening of a resist mask, its configuration, etc. are not limited to the configuration of an example that what is necessary is just to design so that it may become less than [more than abbreviation 2 4.5] in the shoulder upper part of a sidewall spacer. Moreover, it is Si 3N4 in the self aryne contact structure which shares a sidewall spacer and an etching stopper layer, i.e., a sidewall spacer. this invention can be applied when forming. moreover, a thing applicable not only to two or more gate inter-electrode self aryne contacts but formation of the self aryne contact expected to for example, a gate electrode and the semiconductor substrate between LOCOS(s) if it elaborates on the technical thought of this invention -- obvious -- it is . Moreover, various change is possible for the plasma etching method, equipment, etc. It is desirable from a viewpoint of homogeneity, a low damage, or a throughput to use etching systems which may generate plasma with high ion density, such as an efficient consumer response plasma etching system, an inductive-coupling plasma etching system, and a helicon wave plasma etching system, especially as a plasma etching system.
[0038]

[Effect of the Invention] According to the manufacture method of the semiconductor device of this invention, in self aryne contact hole processing using the etching stopper layer, the etch selectivity of a layer insulation film and an etching stopper layer can be improved so that clearly from the above explanation. Since it is not necessary to depend for etch selectivity on superfluous polymer deposition, there is also no fear of the throughput fall by etching-rate reduction. Since etching of a sidewall spacer or an offset insulator layer was prevented and the distance between a gate electrode and a contact plug was fully secured by this, isolation voltage improved and it became possible to offer the manufacture method of the reliable semiconductor device integrated highly.

[Translation done.]

NOTICES *

1. This document has been translated by computer.So the translation may not reflect the original precisely.
2. **** shows the word which can not be translated.
3.In the drawings, any words are not translated.

TECHNICAL FIELD [The technical field to which invention belongs] this invention relates to the manufacture method of a semiconductor device of having the process which forms self aryne contact structure with high-reliability, in more detail about the manufacture method of a semiconductor device.

[Translation done.]

PRIOR ART [Description of the Prior Art] the high integration of semiconductor devices, such as LSI, and highly-efficient-izing -- progressing -- following -- a gate electrode and connection -- design rules, such as a hole, are also being reduced to less than [a quarter micron or it] In this semiconductor device, in order to avoid the various troubles which accompany high integration, also in the interlayer connection structure in a multilayer interconnection, much devices are taken on a layout or a process.

[0003] As the example, there are the alignment gap of an aligner and the problem of size deflection at the time of lithography. In the present aligner, the alignment precision gap at the time of mask alignment is the thing of 80nm and a scanning type in a stepper, and is said to be 50nm. for this reason -- for example, detailed contact hole formation gate inter-electrode [two or more] is becoming difficult

[0004] The method thought out in order to solve this problem is self aryne contact (Self Aligned Contact) technology. the connection which attends the impurity diffusion layer of two or more gate inter-electrode semiconductor substrates etc. when self aryne contact forms the sidewall spacer and the etching stopper layer in the sides, such as a gate electrode, -- a hole -- self -- it is the method of carrying out opening conformably The process which carries out alignment of the resist mask which has detailed opening to the connection hole opening schedule section strictly by adoption of self aryne contact becomes unnecessary. Moreover, since it becomes unnecessary [an alignment margin], reduction of a semiconductor chip or cell area is also attained.

[0005] The outline of the manufacture method of the conventional self aryne contact is explained with reference to drawing 5 and drawing 6 . As first shown in drawing 5 (a), the gate insulator layer 2, the gate electrode 3, and the offset insulator layer 4 are formed one by one on the semiconductor substrates 1, such as silicon. next the sidewall cambium (not shown) by the silicon oxide etc. is deposited on the whole surface, whole surface etchback of this is carried out, and it is shown in drawing 5 (b) -- as -- the sidewall spacer 5 -- the side of the gate electrode 3 and the offset insulator layer 4 -- leaving -- further -- the whole surface -- Si 3N4 etc. -- the etching stopper layer 6 is formed in conformal one In addition, before and after the formation process of the sidewall spacer 5, an impurity diffusion layer (not shown) is formed at the semiconductor substrate 1. As shown in drawing 5 (c) after this, the layer insulation films 7, such as a silicon oxide, are formed in the whole surface, and patterning of the resist mask 8 further for self aryne contact openings is carried out. The exact alignment at the time of exposure of resist mask 8 patterning does not need strict nature so much. As furthermore shown in drawing 6 (d), anisotropic etching of the layer insulation film 7 is carried out by using the resist mask 8 as an etching mask. Under the present circumstances, opposite Si 3N4 The high etching conditions of a selection ratio are adopted and etching is stopped on the etching stopper layer 6. Then, as shown

in drawing 6 (e), the exposed etching stopper layer 6 is removed by wet etching, ionicity weak dry etching, etc., and the self aryne contact hole 9 which attends the impurity diffusion layer of the semiconductor substrate 1 is completed.

[0006] The outline plan of self aryne contact hole 9 portion which removed the etching stopper layer 6 and was completed is shown in drawing 6 (e). It has the position and width of face which were regulated by the self-adjustment target with the sidewall spacer 5, and opening of the pars basilaris ossis occipitalis of the self aryne contact hole 9 can also be considered as the minute opening width of face below the resolution limit of lithography.

[Translation done.]

EFFECT OF THE INVENTION [Effect of the Invention] According to the manufacture method of the semiconductor device of this invention, in self aryne contact hole processing using the etching stopper layer, the etch selectivity of a layer insulation film and an etching stopper layer can be improved so that clearly from the above explanation. Since it is not necessary to depend for etch selectivity on superfluous polymer deposition, there is also no fear of the throughput fall by etching-rate reduction. Since etching of a sidewall spacer or an offset insulator layer was prevented and the distance between a gate electrode and a contact plug was fully secured by this, isolation voltage improved and it became possible to offer the manufacture method of the reliable semiconductor device integrated highly.

[Translation done.]

TECHNICAL PROBLEM [Problem(s) to be Solved by the Invention] The technical key point in a self aryne contact process is Si 3N4 used as an etching stopper layer. SiO2 with the receiving high selection ratio It is adoption of etching conditions. Etching removal of the etching stopper layer is carried out to this selection ratio being insufficient, the sidewall spacer exposed from the etching stopper layer and an offset insulator layer carry out film decrease, and, as a result, the fall of a contact plug / gate inter-electrode pressure-proofing and faults, such as a short circuit, arise.
[0008] SiO2 / Si 3N4 As a method of raising the etch selectivity of a between, the method using the mixed gas which added CO is in the etching gas of CF system as reported to the collection p537 of the 41st applied-physics relation union lecture meeting (1994 spring annual conventions) lecture drafts, and lecture number 29 p-ZF -2. this -- SiO2 the ionicity in anisotropic etching -- to some extent -- suppressing -- mainly -- Si 3N4 a top -- carbon -- the protective coat by rich CF system polymer -- depositing -- SiO2 The fall of an etching rate is the method of obtaining a selection ratio, by adopting a high-density plasma etching system.
[0009] However, in the anisotropic etching of self aryne contact, there is a specific problem that it is large, namely, the etching rate of a selection ratio of the etching stopper layer 6 of the up shoulder of the sidewall spacer 5 is small as compared with the etching rate of the etching stopper layer 6 of a flat part. This is because sputtering removal of the CF system polymer which should be deposited on a sidewall spacer 5 up shoulder is carried out preferentially, when the vertical-incidence nature of ion is raised for anisotropic etching. This cause is made because, as for the sputtering efficiency by ion, an ion incident angle serves as the maximum at 40-60 degrees. If the ion mode nature in anisotropic etching is weakened or too much polymer deposition is formed in order to improve the selection ratio in etching stopper layer 6 portion on a sidewall spacer 5 up shoulder, the problem that etching stops at the contact hole bottom of a high aspect ratio will newly occur.
[0010] Let it be the technical problem for this invention to solve the trouble of these conventional technology in the manufacture method of a semiconductor device including the self aryne contact formation process mentioned above. That is, the technical problem of this invention is Si 3N4 as an etching stopper layer. It sets to the manufacture method of a semiconductor device including used self aryne contact processing, and they are SiO2 / Si3N4. It is improving the selection ratio of a between and offering the manufacture method of the semiconductor device in which the high anisotropic etching of a throughput is possible. Moreover, another technical problem of this invention is offering the manufacture method of a semiconductor device of having reliable self aryne contact structure without fear, such as a fall of isolation voltage, and a short circuit.

[Translation done.]

MEANS [Means for Solving the Problem] this invention is made in order to attain the technical technical problem mentioned above. Namely, the process at which the manufacture method of the semiconductor device of this invention forms two or more gate electrodes through a gate insulator layer on a semiconductor substrate, All over two or more this gate insulator layer top and gates electrode top, anisotropic etching of the process and sidewall cambium which form a sidewall cambium is carried out. The process which forms a sidewall spacer in two or more previous gate electrode sides, The process which forms an etching stopper layer in the whole surface, the process which forms a layer insulation film on this etching stopper layer, The process which forms the resist mask which has opening which attends two or more previous gate inter-electrode semiconductor substrates and sidewall spacers on this layer insulation film, and this resist mask are used as an etching mask. In the manufacture method of a semiconductor device of having the process which carries out anisotropic etching of the layer insulation film at least, and carries out opening of the self aryne contact hole An aspect ratio also including the thickness of a resist mask of this self aryne contact hole is characterized by being less than [more than abbreviation 2 4.5] in a part for a sidewall spacer up shoulder.
[0012] The manufacture method of the semiconductor device of this invention may set like 1 operative condition, and the opening flat-surface configuration of this resist mask may have two or more openings. Moreover, in the manufacture method of the semiconductor device of this invention, while an etching stopper layer contains a silicon-nitride layer, a layer insulation film can be preferably applied, when a silicon-oxide layer is included.
[0013] It moves to explanation of the operation to the next. this invention person is SiO2 / Si 3N4 used as the key point in the anisotropic etching of self aryne contact. As a result of advancing examination wholeheartedly about the selection ratio of a between, the substantial aspect ratio including the thickness of the resist mask in a self aryne contact hole portion other than etching conditions, such as selection of a type of gas, found out influencing a selection ratio greatly. This relation is explained with reference to drawing 4 .
[0014] Drawing 4 is SiO2 / Si 3N4 at the time of self aryne contact opening. It is the graph which shows the selection ratio of a between, and the relation of an aspect ratio. Etching adopts a magnetron RIE system and etching gas is C4 F8 as CF system gas. The mixed gas containing CO was used. Moreover, the aspect ratio said here is the value of h/a which **(ed) the value of the distance h from a part for the up shoulder of the sidewall spacer 5 of the self aryne contact hole 9 (the portion S enclosed with the dotted-line circle of drawing 4) to the front face of the resist mask 8 with the value of the opening width of face a of the resist mask 8.
[0015] It turns out that an aspect ratio can attain 20 or more etch selectivity in not more than more than abbreviation 2 4.5 so that clearly from the graph of drawing 4 . If these high

selection-ratio conditions are used, before dirty-off of the etching stopper layer 6 of S portion is carried out, it is possible enough to remove the layer insulation film 7 of self aryne contact hole 9 bottom without a residue. Control of the value of this aspect ratio h/a is possible by the design of the diameter a of opening of the resist mask 8, thickness, or the thickness of a layer insulation film. Moreover, an aspect ratio becomes less than two from the relation of device structure. In this case, what is necessary is to make the opening flat-surface configuration of the resist mask 8 into plurality, and just to control a substantial aspect ratio in the range not more than more than abbreviation 2 4.5 by reducing the diameter a of opening.

[Translation done.]

EXAMPLE [Example] Hereafter, with reference to an accompanying drawing, it explains about the concrete example of this invention. In addition, the same reference mark shall be given to the same component as the inside of drawing 5 with which explanation of the conventional technology was presented, and drawing 6 .

[0017] Example 1 this example uses the opening flat-surface configuration of a resist mask as single opening, controls an aspect ratio by controlling the thickness of a resist mask, and is SiO2 / Si 3N4. It is the example which improved the selection ratio of a between, and the drawing 1 reference is carried out and this is explained.

[0018] The structure of the processed substrate adopted by this example is the same as that of what was shown by drawing 5 (c) with which explanation of the conventional example was presented fundamentally. Namely, as the processed substrate adopted by this example is shown in drawing 1 (a) On the semiconductor substrates 1, such as silicon, for example, by thermal oxidation The gate insulator layer 2 and n+ which were formed in the thickness of 10nm two or more gate electrodes 3 with a thickness of 500nm it is thin from polycrystal silicon, and SiO2 from -- SiO2 of thickness with a width of face of 250nm formed in the side of the offset insulator layer 4 with a thin thickness of 500nm, the gate electrode 3, and the offset oxide film 4 from -- the becoming sidewall spacer 5 -- Were formed in the whole surface of reduced pressure CVD. Si 3N4 from -- SiO2 formed all over the etching stopper layer 6 with a thin thickness of 50nm It consists of a layer insulation film 7 which consists of a PSG etc., and a resist mask 8 for self aryne contact openings formed in the thickness of 1.2 micrometers. Patterning of the single opening of the diameter of 0.8 micrometer which attends the semiconductor substrate 1 between the sidewall spacer 5 and the sidewall spacer 5 is carried out to this resist mask, for example. The exact alignment at the time of exposure of this resist mask 8 patterning does not need strict nature so much. The thickness of the layer insulation film 7 is 800nm in the flat part for example, on the offset insulator layer 4, and flattening of the front face may be carried out by reflow heat treatment, chemical mechanical polishing, etc. Moreover, the distance between the gate electrodes 3 which plurality adjoins is 850nm.

[0019] As the processed substrate of this structure was etched two stages by the magnetron RIE system and it was shown in drawing 1 (b) according to the following etching conditions, the self aryne contact hole 9 was formed.

1st-step etching (etching of the layer insulation film 7) C4 F8 Flow rate 10 sccm CO flow rate 150 sccm Ar flow rate 200 sccm Gas pressure 5.3 Pa RF power 1600 W (13.56MHz) Processed substrate temperature The step [20 ** / 2nd step] etching (etching of the etching stopper layer 6) CHF3 Flow rate 20 sccm O2 Flow rate 20 sccm Gas pressure 2.7 Pa RF power 500 W (13.56MHz)

Processed substrate temperature 20 ** [0020] When the processed substrate adopted by this example forms the thickness of the resist mask 8 comparatively thickly with 1.2 micrometers, the aspect ratio of the self aryne contact hole 9 is designed in the sidewall spacer 6 shoulder upper part including the thickness of the resist mask 8 so that it may be set to 2.5. Therefore, SiO2/Si 3N4 in this portion The etch selectivity of a between is the highest field so that clearly from the graph of drawing 4 .

[0021] For this reason, also in the shoulder upper part of the sidewall spacer 5 which spatter out is the easiest to be carried out in the 1st-step etching, it does not generate, therefore neither the sidewall spacer 5 nor the offset insulator layer 4 carries out film decrease of the fault the etching stopper layer 6 disappears. The 2nd-step etching is ended and the flat-surface configuration of self aryne contact hole 9 portion after exfoliating the resist mask 8 is shown in drawing 1 (c). The semiconductor substrate 1 and the sidewall spacer 5 are exposed to self aryne contact hole 9 base. Then, the contact plug and the upper wiring which are not illustrated according to a conventional method are formed.

[0022] They are SiO2 / Si 3N4 by optimizing the thickness of the resist mask of a single opening flat-surface configuration according to this example. It is possible to manufacture the semiconductor device which has the self aryne contact hole which raised the etch selectivity of a between and was excellent in the configuration.

[0023] By using the opening flat-surface configuration of a resist mask as opening of the shape of two or more ellipse, example 2 this example controls an aspect ratio, and is SiO2 / Si 3N4. It is the example which improved the selection ratio of a between, and the drawing 2 reference is carried out and this is explained.

[0024] The structure of the processed substrate shown in drawing 2 (a) adopted by this example is the same as that of what was shown by drawing 5 (c) with which explanation of the conventional example was presented fundamentally. that is On the semiconductor substrates 1, such as silicon, by thermal oxidation The gate insulator layer 2 and n+ which were formed in the thickness of 10nm two or more gate electrodes 3 with a thickness of 500nm it is thin from polycrystal silicon, and SiO2 from -- SiO2 of thickness with a width of face of 200nm formed in the side of the offset insulator layer 4 with a thin thickness of 300nm, the gate electrode 3, and the offset oxide film 4 from -- the becoming sidewall spacer 5 -- SiO2 formed all over the etching stopper layer 6 with a thickness of 50nm formed in the whole surface of reduced pressure CVD By PSG etc. It consists of a formed layer insulation film 7 and a resist mask 8 for self aryne contact openings formed in the thickness of 0.5 micrometers. For example, it attends the semiconductor substrate 1 between the sidewall spacer 5 and the sidewall spacer 5, patterning of the two ellipse openings of the diameter of 0.8 micrometerx0.3 micrometer is carried out in parallel, and the slit between two openings has become 0.2 micrometers at this resist mask 8. The resist mask of this configuration can be formed with for example, a chemistry amplification resist and excimer laser lithography. The exact alignment at the time of exposure of this resist mask 8 patterning does not need strict nature so much. The thickness of the layer insulation film 7 is 400nm in the flat part for example, on the offset insulator layer 4. Moreover, the distance between the gate electrodes 3 which plurality adjoins is 1.0 micrometers.

[0025] The processed substrate of this structure was etched two stages according to the following etching conditions by the magnetron RIE system.

1st-step etching (etching of the layer insulation film 7) C4 F8 Flow rate 10 sccm CO flow rate 150 sccm Ar flow rate 200 sccm Gas pressure 5.3 Pa RF power 1600 W (13.56MHz)

Processed substrate temperature The step [20 ** / 2nd step] etching (etching of the etching stopper layer 6) CHF3 Flow rate 20 sccm O2 Flow rate 20 sccm Gas pressure 2.7 Pa RF power 500 W (13.56MHz)
Processed substrate temperature 20 ** [0026] When the processed substrate adopted by this example divides the opening configuration of the resist mask 8 into plurality, the aspect ratio of the direction of a minor axis of self aryne contact hole 9 opening including the thickness of the resist mask 8 is designed so that it may be set to 3.0 in the shoulder upper part of the sidewall spacer 5. Therefore, SiO2/Si 3N4 in this portion The etch selectivity of a between shows the highest value so that clearly from the graph of drawing 4 .
[0027] For this reason, also in the shoulder upper part of the sidewall spacer 5 which spatter out is the easiest to be carried out in the 1st-step etching, it does not generate, therefore neither the sidewall spacer 5 nor the offset insulator layer 4 carries out film decrease of the fault the etching stopper layer 6 disappears. The configuration of self aryne contact hole 9 portion after the 1st-step etching end is shown in drawing 2 (b). The etching stopper layer 6 was removed by the 2nd-step weak etching in ion mode after this, the resist mask 8 was exfoliated further, and the self aryne contact hole 9 was completed. The flat-surface configuration of self aryne contact hole 9 portion is shown in drawing 2 (c). The semiconductor substrate 1 and the sidewall spacer 5 are exposed to two self aryne contact hole bases of an ellipse.
[0028] The contact plug and the upper wiring which are not illustrated according to a conventional method after this are formed. Although the pillar of the slit-like layer insulation film 7 remains in the self aryne contact hole 9, unless trouble is caused to a contact plug and the step coverage at the time of formation of the upper wiring, you may leave as it is. Moreover, after isotropic etching etc. removes separately, you may form a contact plug and the upper wiring.
[0029] They are SiO2 / Si 3N4 by dividing the opening flat-surface configuration of a resist mask into two or more ellipses according to this example. It is possible to manufacture the semiconductor device which has the self aryne contact hole which raised the etch selectivity of a between and was excellent in the configuration.
[0030] By using the opening flat-surface configuration of a resist mask as concentric circle-like opening, example 3 this example controls an aspect ratio, and is SiO2 / Si 3N4. It is the example which improved the selection ratio of a between, and the drawing 3 reference is carried out and this is explained.
[0031] The structure of the processed substrate shown in drawing 3 (a) adopted by this example is the same as that of what was shown by drawing 5 (c) with which explanation of the conventional example was presented fundamentally. that is On the semiconductor substrates 1, such as silicon, by thermal oxidation The gate insulator layer 2 and n+ which were formed in the thickness of 10nm two or more gate electrodes 3 with a thickness of 500nm it is thin from polycrystal silicon, and SiO2 from -- SiO2 of thickness with a width of face of 200nm formed in the side of the offset insulator layer 4 with a thin thickness of 300nm, the gate electrode 3, and the offset oxide film 4 from -- the becoming sidewall spacer 5 -- SiO2 formed all over the etching stopper layer 6 with a thickness of 50nm formed in the whole surface of reduced pressure CVD By PSG etc. It consists of a formed layer insulation film 7 and a resist mask 8 for self aryne contact openings formed in the thickness of 0.5 micrometers.
[0032] As this resist mask 8 is shown in the opening flat-surface configuration shown in drawing 3 (b), it has circular opening with a diameter of 0.8 micrometers expected to the semiconductor substrate 1 between the sidewall spacer 5 and the sidewall spacer 5, and with a diameter of 0.2

micrometers resist pillar 8a is formed in the shape of a concentric circle. Therefore, concentric circle-like resist mask 8 opening width of face is 0.3 micrometers. The resist mask of this configuration can also be formed with a chemistry amplification resist and excimer laser lithography. The exact alignment at the time of exposure of this resist mask 8 patterning does not need strict nature so much. The thickness of the layer insulation film 7 is 400nm in the flat part for example, on the offset insulator layer 4. Moreover, the distance between the gate electrodes 3 which plurality adjoins is 1.0 micrometers.

[0033] As the processed substrate of this structure was etched two stages by the magnetron RIE system and it was shown in drawing 3 (c) according to the following etching conditions, the self aryne contact hole 9 was formed.

1st-step etching (etching of the layer insulation film 7) C4 F8 Flow rate 10 sccm CO flow rate 150 sccm Ar flow rate 200 sccm Gas pressure 5.3 Pa RF power 1600 W (13.56MHz) Processed substrate temperature The step [20 ** / 2nd step] etching (etching of the etching stopper layer 6) CHF3 Flow rate 20 sccm O2 Flow rate 20 sccm Gas pressure 2.7 Pa RF power 500 W (13.56MHz)

Processed substrate temperature 20 ** [0034] When the processed substrate adopted by this example makes the opening configuration of the resist mask 8 the shape of a concentric circle, the radial aspect ratio of the self aryne contact hole 9 including the thickness of the resist mask 8 is designed so that it may be set to 3.0 in the shoulder upper part of the sidewall spacer 5. Therefore, SiO2 / Si 3N4 in this portion The highest value is shown that the etch selectivity of a between is clear from the graph of drawing 4 .

[0035] For this reason, also in the shoulder upper part of the sidewall spacer 5 which spatter out is the easiest to be carried out in the 1st-step etching, it does not generate, therefore neither the sidewall spacer 5 nor the offset insulator layer 4 carries out film decrease of the fault the etching stopper layer 6 disappears. Then, the resist mask 8 after removing the etching stopper layer 6 is exfoliated by the 2nd-step etching, and the contact plug and the upper wiring which are not illustrated according to a conventional method are formed. Although the pillar of the circular layer insulation film 7 remains in the self aryne contact hole 9, unless trouble is caused to a contact plug and the step coverage at the time of formation of the upper wiring, you may leave as it is. Moreover, after isotropic etching etc. removes separately, you may form a contact plug and the upper wiring.

[0036] They are SiO2 / Si 3N4 by making the opening flat-surface configuration of a resist mask into the shape of a concentric circle according to this example. It is possible to manufacture the semiconductor device which has the self aryne contact hole which raised the etch selectivity of a between and was excellent in the configuration.

[0037] As mentioned above, although the example of three examples explained this invention in detail, this invention is not limited to these examples at all. That is, the thickness of the resist mask in an example or a layer insulation film, the diameter of opening of a resist mask, its configuration, etc. are not limited to the configuration of an example that what is necessary is just to design so that it may become less than [more than abbreviation 2 4.5] in the shoulder upper part of a sidewall spacer. Moreover, it is Si 3N4 in the self aryne contact structure which shares a sidewall spacer and an etching stopper layer, i.e., a sidewall spacer. this invention can be applied when forming. moreover, a thing applicable not only to two or more gate inter-electrode self aryne contacts but formation of the self aryne contact expected to for example, a gate electrode and the semiconductor substrate between LOCOS(s) if it elaborates on the technical thought of

this invention -- obvious -- it is . Moreover, various change is possible for the plasma etching method, equipment, etc. It is desirable from a viewpoint of homogeneity, a low damage, or a throughput to use etching systems which may generate plasma with high ion density, such as an efficient consumer response plasma etching system, an inductive-coupling plasma etching system, and a helicon wave plasma etching system, especially as a plasma etching system.

[Translation done.]

DESCRIPTION OF DRAWINGS [Brief Description of the Drawings]
[Drawing 1] It is the outline cross section and plan which explain the process of the example 1 which applied this invention in order of the process.
[Drawing 2] It is the outline cross section and plan which explain the process of the example 2 which applied this invention in order of the process.
[Drawing 3] It is the outline cross section and plan which explain the process of the example 3 which applied this invention in order of the process.
[Drawing 4] An aspect ratio including the resist mask, and SiO2 / Si 3N4 It is the graph which shows the etch selectivity of a between.
[Drawing 5] It is the outline cross section showing the process of the first half of the general formation process of self aryne contact.
[Drawing 6] It is the outline cross section and plan showing the process of the second half of the general formation process of self aryne contact.
[Description of Notations]
1 [-- A gate electrode, 4 / -- An offset insulator layer, 5 / -- A sidewall spacer, 6 / -- An etching stopper layer, 7 / -- A layer insulation film, 8 / -- A resist mask, 8a / -- A resist pillar, 9 / -- A self aryne contact hole, S / -- The shoulder upper part of a sidewall spacer] -- A semiconductor substrate, 2 -- A gate insulator layer, 3

JAPANESE [JP,09-320980,A]

CLAIMS DETAILED DESCRIPTION TECHNICAL FIELD PRIOR ART EFFECT OF THE INVENTION TECHNICAL PROBLEM MEANS EXAMPLE DESCRIPTION OF DRAWINGS DRAWINGS

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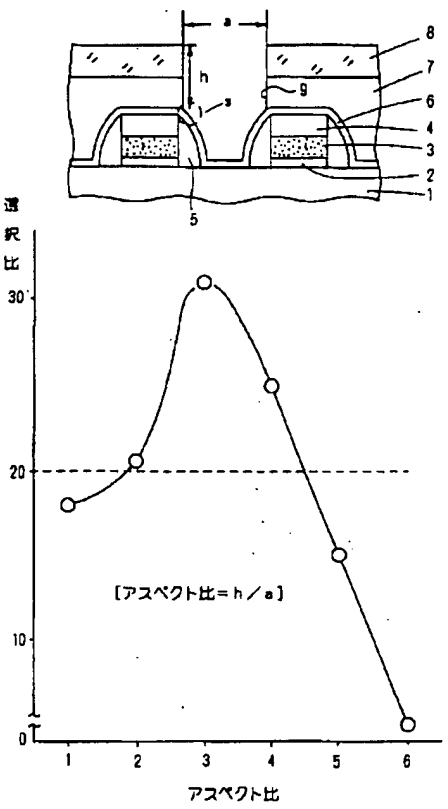
CLAIMS

[Claim(s)]

Drawing selection

[Representative drawing]



[Translation done.]

JAPANESE [JP,09-320980,A]

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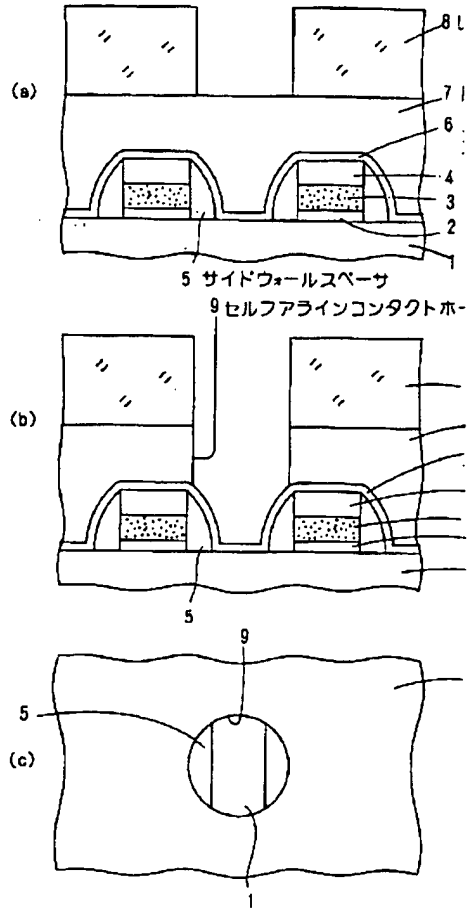
Drawing selection

drawing 1



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CLAIMS

[Claim(s)]
[Claim 1] The process which forms two or more gate electrodes through a gate insulator layer on a semiconductor substrate, All over [aforementioned-on aforementioned gate insulator layer] two or more gate electrode top, anisotropic etching of the process and the aforementioned sidewall cambium which form a sidewall cambium is carried out. The process which forms a sidewall spacer in two or more aforementioned gate electrode sides, The process which forms an etching stopper layer in the whole surface, the process which forms a layer insulation film on the aforementioned etching stopper layer, The process and the aforementioned resist mask which form the resist mask which has opening which attends gate inter-electrode the semiconductor substrate and sidewall spacer of the aforementioned plurality on the aforementioned layer insulation film are used as an etching mask. In the

[Translation done.]

JAPANESE [JP,09-320980,A]

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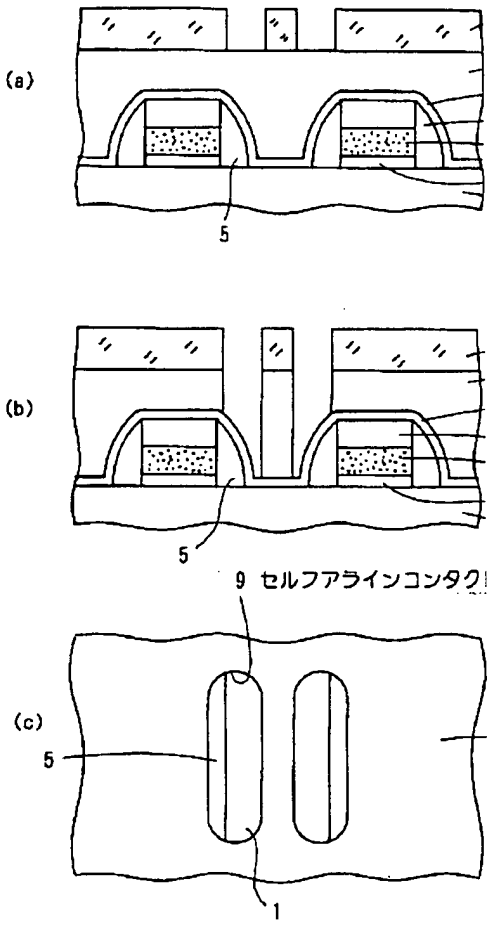
CLAIMS

[Claim(s)]
[Claim 1] The process which forms two or more gate electrodes through a gate insulator layer on a semiconductor substrate, All over [aforementioned-on aforementioned gate insulator layer] two or more gate electrode top, anisotropic etching of the process and the aforementioned sidewall cambium which form a sidewall cambium is carried out. The process which forms a sidewall spacer in two or more aforementioned gate electrode sides, The process which forms an etching stopper layer in the whole surface, the process which forms a layer insulation film on the aforementioned etching stopper layer, The process and the aforementioned resist mask which form the resist mask which has opening which attends gate inter-electrode the semiconductor substrate and sidewall spacer of the aforementioned plurality on the aforementioned layer insulation film are used as an etching mask. In the

Drawing selection
drawing 2



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JAPANESE [JP,09-320980,A]

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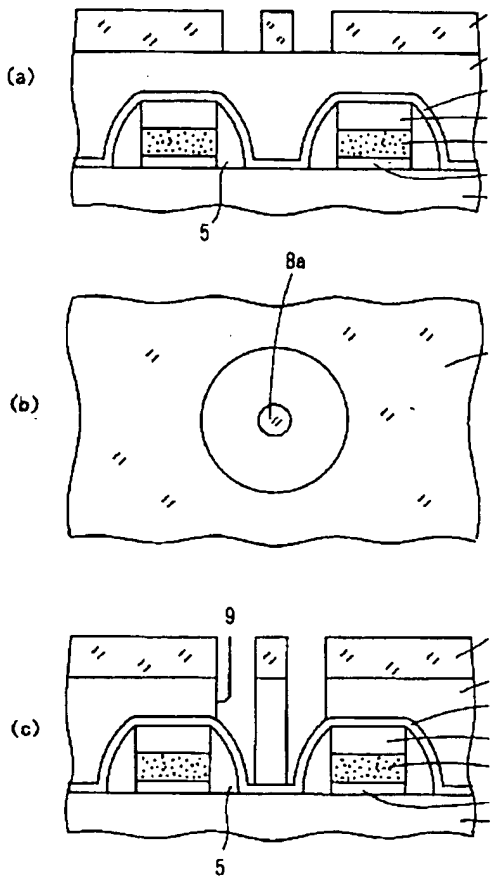
Drawing selection

drawing 3



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CLAIMS

[Claim(s)]
[Claim 1] The process which forms two or more gate electrodes through a gate insulator layer on a semiconductor substrate, All over [aforementioned-on aforementioned gate insulator layer] two or more gate electrode top, anisotropic etching of the process and the aforementioned sidewall cambium which form a sidewall cambium is carried out. The process which forms a sidewall spacer in two or more aforementioned gate electrode sides, The process which forms an etching stopper layer in the whole surface, the process which forms a layer insulation film on the aforementioned etching stopper layer, The process and the aforementioned resist mask which form the resist mask which has opening which attends gate inter-electrode the semiconductor substrate and sidewall spacer of the aforementioned plurality on the aforementioned layer insulation film are used as an etching mask. In the

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JAPANESE [JP,09-320980,A]

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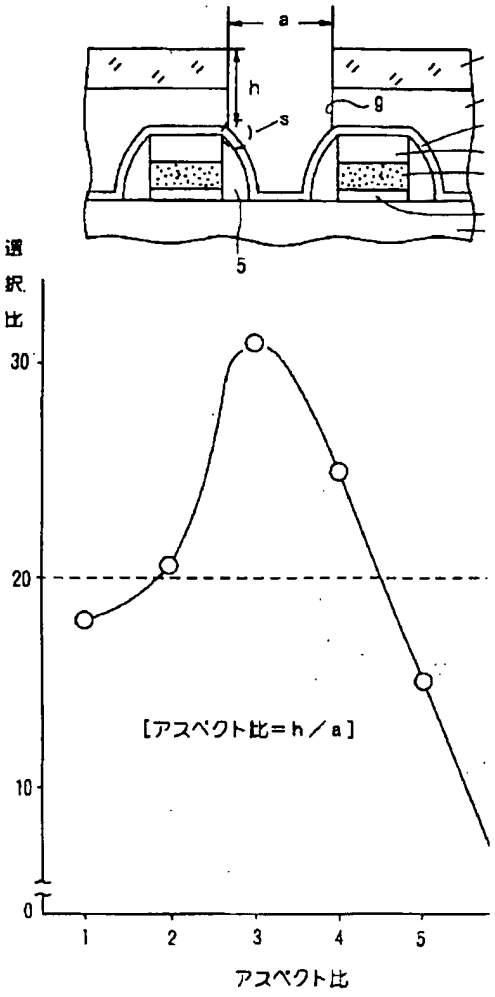
CLAIMS

[Claim(s)]
[Claim 1] The process which forms two or more gate electrodes through a gate insulator layer on a semiconductor substrate, All over [aforementioned-on aforementioned gate insulator layer] two or more gate electrode top, anisotropic etching of the process and the aforementioned sidewall cambium which form a sidewall cambium is carried out. The process which forms a sidewall spacer in two or more aforementioned gate electrode sides, The process which forms an etching stopper layer in the whole surface, the process which forms a layer insulation film on the aforementioned etching stopper layer, The process and the aforementioned resist mask which form the resist mask which has opening which attends gate inter-electrode the semiconductor substrate and sidewall spacer of the aforementioned plurality on the aforementioned layer insulation film are used as an etching mask. In the

Drawing selection
drawing 4



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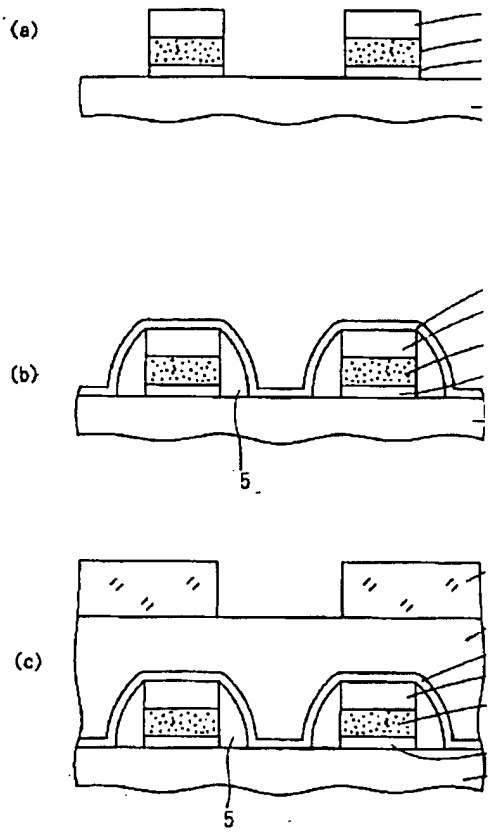
CLAIMS

[Claim(s)]
[Claim 1] The process which forms two or more gate electrodes through a gate insulator layer on a semiconductor substrate, All over [aforementioned-on aforementioned gate insulator layer] two or more gate electrode top, anisotropic etching of the process and the aforementioned sidewall cambium which form a sidewall cambium is carried out. The process which forms a sidewall spacer in two or more aforementioned gate electrode sides, The process which forms an etching stopper layer in the whole surface, the process which forms a layer insulation film on the aforementioned etching stopper layer, The process and the aforementioned resist mask which form the resist mask which has opening which attends gate inter-electrode the semiconductor substrate and sidewall spacer of the aforementioned plurality on the aforementioned layer insulation film are used as an etching mask. In the

Drawing selection
drawing 5



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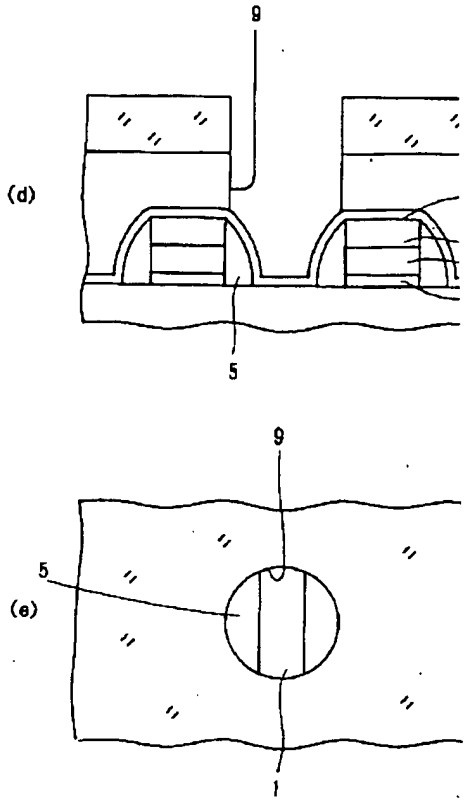
CLAIMS

[Claim(s)]
[Claim 1] The process which forms two or more gate electrodes through a gate insulator layer on a semiconductor substrate, All over [aforementioned-on aforementioned gate insulator layer] two or more gate electrode top, anisotropic etching of the process and the aforementioned sidewall cambium which form a sidewall cambium is carried out. The process which forms a sidewall spacer in two or more aforementioned gate electrode sides, The process which forms an etching stopper layer in the whole surface, the process which forms a layer insulation film on the aforementioned etching stopper layer, The process and the aforementioned resist mask which form the resist mask which has opening which attends gate inter-electrode the semiconductor substrate and sidewall spacer of the aforementioned plurality on the aforementioned layer insulation film are used as an etching mask. In the

Drawing selection
drawing 6



[Translation done.]